Loading Instruction Set on to uZed EEPROM

SDK = Software Design Kit

uZed = Avnet development kit consisting of Zynq SOC and peripherals.

Workspace = Local Directory consisting of the instructions for the FPGA and processor on the Zynq

Zynq = Xilinx System on a Chip. This is the name of a large family of chips, where we have utilized only the Z010 and Z020 chips.

1. Identify the instruction set for the current project.
   1. Note the Zynq Chip set Z010 or Z020. The chip set is explicitly linked to the project.
   2. Note the software version for the operations required.
   3. LunaH software runs with Xilinx 2014.1- this is primarily due to licensing owned by RMD
   4. SINGR requires Ethernet for operation, and the software uses SDK 2015.3
   5. The instruction sets are deposited on GitHub
   6. The instruction sets consist of:
      1. a hardware platform (example: ../hw\_platform\_0/)
      2. Board support package (example: ../standalone\_bsp\_0/)
      3. Software package (example: ../Lunah\_DevKit\_v1.0\_2014\_1/)
2. Define the “workspace” on your local computer, which is downloading or copying the instruction set to a specified folder location.
3. Start Xilinx SDK (note to use the appropriate SDK version).
4. At the startup of the SDK, define the workspace as the folder location of your instruction set.
5. Import Files:
   1. File > Import > General folder > Existing projects into workspace
   2. Click next, then browse to the workspace you defined
   3. Select Add projects to working sets
      1. The instruction sets should populate under projects.
      2. Make sure they are selected.
   4. Select “Copy projects into workspace”
   5. Select “Add project to working sets”
   6. Click Finish
6. Close the Welcome Tab, the Project Explore should be visible.
7. Solve the two errors after the SDK has loaded.
   1. In the Project Explorer Right Click on Board Support Package (ex: standalone\_bsp\_0)
      1. Select Re-generate BSP sources
   2. In the Project Explorer Right click on Software (ex: Lunah\_DevKit\_v1.0\_2014\_1)
      1. Select Generate linker script > generate
   3. There should be 8 warnings and 2 infos at the end of this process
8. Make the First Stage Bootloader
   1. File > New > Application Project
   2. Type In Project Name (example: MZ\_FSBL)
   3. Click Next
   4. Select Zynq FSBL
   5. Click Finish
9. The First Stage bootloader files will be generated (example: MZ\_FSBL and MZ\_FSBL\_bsp)
10. Set FSBL and Software for Release
    1. Right Click on FSBL (example: MZ\_FSBL)
    2. Select Build Configurations > Set Active > Release
    3. Right Click on Software (example: Lunah\_DevKit\_v1.0\_2014\_1)
    4. Select Build Configurations > Set Active > Release
11. Build the both the FSBL and Software projects by clicking on the Hammer Icon for each.
12. Create the Bootimage:
    1. Xilinx Tools > Create Zynq Boot Image
    2. Create New BIF file
       1. Browse to the Software folder (example: Lunah\_DevKit\_v1.0\_2014\_1)
       2. Create New Folder called “bootimage”
       3. Set filename to bootimage.bif in that folder
       4. Under boot image partitions add:
          1. Delete any existing file paths
          2. Click Add > Select FSBL.elf file (ex: MZ\_FSBL.elf) from the release folder of FSBL> Set the Partition type as “bootloader”
          3. Click Add > Select bitstream from the hardware platform   
             (example: ..\hw\_platform\_0\design\_1\_wrapper.bit) >   
             Set the Partition type as “datafile”
          4. Click Add > Select the software release   
             (example: Lunah\_DevKit\_v1.0\_2014\_1\Release\  
             Lunah\_DevKit\_v1.0\_2014\_1.elf) >   
             Set the Partition type as “datafile”
          5. Set the output path as BOOT.mcs in the bootimage folder created above.
13. Program the EEPROM
    1. Connect the board (uZed) to the computer via the JTag cable (Digilent JTAG-HS3 Rev. A)
    2. Select Xilinx Tools > Program Flash
    3. Set Image File as BOOT.mcs generate in previous step.
    4. Click Program
    5. Note the comments in console window, and the operation is completed and successful with it reports “Flash Operation Successful”
    6. A red LED will be lit on the uZed board.
    7. Power cycle the board or press the reset button
    8. A blue LED will be lite if the system boot was successful.